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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,440	11/29/2005	Peter John Miller	KILBU P-74/500728	7566

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REED SMITH, LLP
ATTN: PATENT RECORDS DEPARTMENT
599 LEXINGTON AVENUE, 29TH FLOOR
NEW YORK, NY 10022-7650

EXAMINER	
GAMI, TEJAL	
ART UNIT	**PAPER NUMBER**
2121	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/522,440	MILLER ET AL.	
	Examiner	Art Unit	
	Tejal J. Gami	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The prior art must be listed on a form PTO-892, PTO-1449, PTO /SB /08A or 08B, or PTO /SB /42 (or on a form having format equivalent to one of these forms). These forms must be properly completed. See MPEP § 2657.

Claim Objections

2. Claims 1, 12-13, 16, 19, 22, 25-26, and 28 are objected to because of the following informalities:

Claims 1, 16, 19, 26 : Various periods have been placed incorrectly in the claim. There should be a period placed only at the end of the claim.

Claim 12, Line 2: The placement of the semicolon is grammatically incorrect.

Claim 12, Line 5: The ":" should be removed.

Claim 12, Line 6: The "..." should be removed.

Claim 13, Line 5: The ".." should be removed.

Claim 19, Line 7: The words "to a to a" should read "to a".

Claim 22, Line 2: The word "n1onitoring" should read "monitoring".

Claim 25, Line 1: The ":" should be removed.

Claim 26, Line 7: The apostrophe and ":" should be removed.

Claim 28, Line 3: The word "starling" should read "starting".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3-4, 12-13, 19-20, and 26-28 recite the limitation "the system". There is insufficient antecedent basis for this limitation in the claim. The claim discloses an electronic system and fault-monitoring system.

5. Claim 3, 12, 19, and 26 recite the limitation "the generation". There is insufficient antecedent basis for this limitation in the claim.

6. Claims 14-18 recite the limitation "method". There is insufficient antecedent basis for this limitation in the claim. A method claim cannot depend from a system claim.

7. Claims 20 and 22 recite the limitation "the processor". There is insufficient antecedent basis for this limitation in the claim.

8. Claim 25 recites the limitation "electronic signal" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 19-31 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 19-31 appear to be directed to an abstract idea rather than a practical application of an abstract idea which would produce a "useful, concrete, and tangible result." For example, claims 19 and 26 are merely directed towards storing a record and generating a signal, which may not be held to be a tangible result, and therefore non-statutory subject matter. This claimed subject matter lacks a practical application of a judicial exception since it fails to produce a useful, concrete and tangible result.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-6, 9-15, 18-19, and 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Ulybin (SU 1619279; Translation).

As to independent claim 1, Ulybin discloses an electronic system (e.g., computing system) comprising a plurality of fault-monitoring systems (e.g., several devices) each of which is adapted to output a fault signal (e.g., fault simulation output 13) when an input indicates that the electronic system is in a fault condition associated with the fault-monitoring system (see Page 3), wherein:

the fault-monitoring systems are arranged in a cascade fashion (e.g., cascade of several devices) such that a fault signal output (e.g., fault simulation output 13) from one fault-monitoring system is provided as an input to a subsequent fault-monitoring system in the cascade of fault-monitoring-systems to simulate a fault condition associated with the subsequent fault-monitoring system (see Page 3).

As to independent claim 10, Ulybin discloses a self-test method (e.g., testing the fault tolerance) for an electronic system (e.g., computer system) comprising a plurality of fault-monitoring systems (e.g., several devices) each of which is adapted to output a fault signal (e.g., fault simulation output 13) when an input indicates that the electronic system is in a fault condition associated with the fault-monitoring system (see Page 3), the fault-monitoring systems being arranged in a cascade fashion (e.g., cascade of several devices) such that a fault signal output (e.g., fault simulation output 13) from one fault-monitoring system is provided as an input to a subsequent fault-monitoring system in the cascade of fault-monitoring systems (see Page 3), the method comprising:

inputting the fault signal from one fault-monitoring system to a subsequent fault-monitoring system to simulate a fault condition associated with the subsequent fault-monitoring system (see Page 3).

As to independent claim 19, Ulybin discloses an electronic system (e.g., computing system) comprising at least one fault-monitoring system (e.g., several devices) (see Page 3), the system being arranged to:

place the system into a first fault condition and monitor for the generation of a first fault signal from a first fault-monitoring device, on generation of a first fault signal from the first fault-monitoring device after placing the system into a first fault condition, store a record to this effect in non-volatile memory (see Page 14, Third Paragraph), on subsequent reversion of the system to a to a non-fault condition, check whether the non-volatile memory includes a record of a first fault signal and when the non-volatile memory does not include a record of such a first fault signal on subsequent reversion (e.g., do not match), generate an alarm signal (e.g., when runs at the inputs of comparison block 3 do not match, its output shows the value "0," which is then recorded to trigger 4 by the signal from input 12) (see Page 9, Second Paragraph).

As to independent claim 26, Ulybin discloses a self-test method for an electronic system (e.g., computing system) (see Page 3), the method comprising:

placing the system into a first fault condition and monitoring for the generation of a first fault signal from a fault-monitoring device, on generation of a first fault signal from the fault-monitoring device after placing the system into a first fault condition, storing a record to this effect in non-volatile memory (see Page 14, Third Paragraph), on subsequent reversion of the system to a non-fault condition, checking whether the non-volatile memory includes a record of a first fault signal and when the non-volatile memory does not include a record of such a first fault signal on subsequent commencement (e.g., do not match), generating an alarm signal (e.g., when runs at the inputs of comparison block 3 do not match, its output shows the value "0," which is then recorded to trigger 4 by the signal from input 12) (see Page 9, Second Paragraph).

As to dependent claim 2, Ulybin teaches an electronic system according to claim 1 wherein the output of a final fault-monitoring system in the cascade is used as an indicator of a fault in one of the fault-monitoring systems (see Page 3).

As to dependent claim 3, Ulybin teaches an electronic system according to claim 1, the system further being arranged to:

place the system into a first fault condition and monitor for the generation of a first fault signal from a first fault-monitoring device, on generation of a first fault signal from the fault-monitoring device after placing the system into a first fault condition, to input the first fault signal to the second fault-monitoring device, and in response to an output from a final fault-monitoring device to store a record to this effect in non-volatile memory (see Page 14, Third Paragraph).

As to dependent claim 4, Ulybin teaches an electronic system according to claim 3 wherein, on subsequent reversion of the system to a non-fault condition, the system is arranged to check whether the non-volatile memory includes a record and when the non-volatile memory does not include a record on subsequent reversion (e.g., do not match), generate an alarm signal (e.g., when runs at the inputs of comparison block 3 do not match, its output shows the value "0," which is then recorded to trigger 4 by the signal from input 12) (see Page 9, Second Paragraph).

As to dependent claim 5, Ulybin teaches an electronic system according to claim 1 wherein a first fault-monitoring system is adapted to output a fault signal when the electronic system is placed into a switched-off condition (e.g., with the extended

non-occurrence of the tracked condition in the computing system, the condition will modify automatically) (see Page 10).

As to dependent claim 6, Ulybin teaches an electronic system according to claim 5 wherein the first fault-monitoring system is a watch-dog system (e.g., the frequency of time markers is selected so that it ensures overflow of counter 2 after the period of time specified for fault simulation at one address) (see Page 5, Second Paragraph).

As to dependent claim 9, Ulybin teaches an electronic system according to claim 1 further comprising storing a record of a fault signal output by any of the fault-monitoring systems to enable identification (e.g., address identifiers) of a defective fault-monitoring system (see Page 3).

As to dependent claim 11, Ulybin teaches a self-test method according to claim 10 wherein the output of a final fault-monitoring system in the cascade is used as an indicator of a fault in one of the fault-monitoring systems (see Page 3).

As to dependent claim 12, Ulybin teaches a self-test method according to claim 10, further comprising:

placing the system into a first fault condition and monitoring for the generation of a first fault signal from a first fault-monitoring device, on generation of a first fault signal from the fault-monitoring device after placing the system into a first fault condition, inputting the first fault signal to the second fault-monitoring device, and in response to an output from a final fault-monitoring device storing a record to this effect in non-volatile memory (see Page 14, Third Paragraph).

As to dependent claim 13, Ulybin teaches a self-test method according to claim 12 further comprising, on subsequent reversion of the system to a non-fault condition, checking whether the non-volatile memory includes a record and when the non-volatile memory does not include a record on subsequent reversion (e.g., do not match), generating an alarm signal (e.g., when runs at the inputs of comparison block 3 do not match, its output shows the value "0," which is then recorded to trigger 4 by the signal from input 12) (see Page 9, Second Paragraph).

As to dependent claim 14, Ulybin teaches a self-test method according to claim 1 further comprising outputting a fault signal from the first fault-monitoring system when the electronic system is placed into a switched-off condition (e.g., with the extended non-occurrence of the tracked condition in the computing system, the condition will modify automatically) (see Page 10).

As to dependent claim 15, Ulybin teaches a self-test method according to claim 14 wherein the first fault-monitoring system is a watch-dog system (e.g., the frequency of time markers is selected so that it ensures overflow of counter 2 after the period of time specified for fault simulation at one address) (see Page 5, Second Paragraph).

As to dependent claim 18, Ulybin teaches a self-test method according to claim 1 further comprising storing a record of a fault signal output by any of the fault-monitoring systems to enable identification (e.g., address identifiers) of a defective fault-monitoring system (see Page 3).

As to dependent claim 23, Ulybin teaches an electronic system according to claim 19 further arranged to clear the non-volatile memory of the record once it has

been determined whether or not the non-volatile memory includes a record of a fault signal (see Page 14, Third Paragraph).

As to dependent claim 24, Ulybin teaches an electronic system according to claim 19 further comprising a plurality of fault-monitoring systems, a fault signal output of a first fault-monitoring system being provided as an input to a second fault-monitoring system, such that an input to the second fault-monitoring system simulates a second fault condition (see Page 3).

As to dependent claim 25, Ulybin teaches an electronic signal according to claim 24 wherein the output of a final fault-monitoring system is used as an indicator of an overall fault in one of the fault-monitoring systems (see Page 3).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ulybin (SU 1619279) and further in view of Pierret et al. (U.S. Patent Number 5,079,496).

As to dependent claim 7, Ulybin teaches an electronic system according to claim 5. Ulybin clearly teaches an electronic system, but does not mention a vehicle ignition key. Pierre teaches electronic system is associated with a vehicle and the

electronic system is placed into a switched-off condition by turning an ignition key (see Pierret: Col. 1, Lines 27-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a vehicle ignition key as taught by Pierre to the electronic system of Ulybin because the closed ignition switch enables the battery to be charged (see Pierret: Col. 1, Lines 27-33).

As to dependent claim 16, Ulybin teaches a self-test method according to claim 14. Ulybin clearly teaches an electronic system, but does not mention a vehicle ignition key. Pierre teaches electronic system is associated with a vehicle and the electronic system is placed into a switched-off condition by turning an ignition key (see Pierret: Col. 1, Lines 27-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a vehicle ignition key as taught by Pierre to the electronic system of Ulybin because the closed ignition switch enables the battery to be charged (see Pierret: Col. 1, Lines 27-33).

15. Claims 8, 17, 20-22,and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ulybin (SU 1619279) and further in view of Aslin et al. (U.S. Patent Number 4,943,919).

As to dependent claims 8 and 17, Ulybin teaches an electronic system. Ulybin clearly teaches a second fault-monitoring system has as an input the fault signal from the first fault-monitoring system, the second fault-monitoring system being adapted to output a fault signal (see Ulybin: Page 3), but does not mention an under- or over-voltage condition. Aslin teaches an electronic system experiencing an under- or over-

voltage condition (see Aslin: Col. 12, Lines 38-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized voltage condition as taught by Aslin to the fault-monitoring system of Ulybin because the analog discrete fault data is analyzed in the same manner as the digital fault data (see Aslin: Col. 12, Lines 47-49).

As to dependent claim 20, Ulybin teaches an electronic system according to claim 19. Ulybin clearly teaches placing of the system into a first fault condition and subsequent reversion of the system to a non-fault condition (see Ulybin: Page 14, Third Paragraph), but does not mention a processor. Aslin teaches operation of a processor (see Aslin: Col. 6, Lines 34-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a processor as taught by Aslin to the fault condition of Ulybin because the consolidation module generates an isolated fault from the fault data by screening out cascaded faults and consolidating multiple faults (see Aslin: Col. 6, Lines 39-45).

As to dependent claim 21, Ulybin teaches an electronic system according to claim 19. Ulybin clearly teaches the fault monitoring device (see Ulybin: Page 3), but does not mention a voltage detector. Aslin teaches a voltage detector which generates a fault signal when an over-voltage occurs (see Aslin: Col. 12, Lines 38-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a voltage detector as taught by Aslin to the fault monitoring device of Ulybin because the analog discrete fault data is analyzed in the same manner as the digital fault data (see Aslin: Col. 12, Lines 47-49).

As to dependent claim 22, Ulybin teaches an electronic system according to claim 19 wherein the fault-monitoring device comprises a device for monitoring the operation and generating a fault signal when a fault with the operation is detected (see Ulybin: Page 3), but does not mention a processor. Aslin teaches operation of a processor (see Aslin: Col. 6, Lines 34-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a processor as taught by Aslin to the fault-monitoring device of Ulybin because the consolidation module generates an isolated fault from the fault data by screening out cascaded faults and consolidating multiple faults (see Aslin: Col. 6, Lines 39-45).

As to dependent claim 27, Ulybin teaches a self-test method according to claim 26. Ulybin clearly teaches the electronic system, wherein the placing of the system into a first fault condition and subsequent reversion of the system to a non-fault condition (see Ulybin: Page 14, Third Paragraph), but does not mention a processor. Aslin teaches operation of a processor (see Aslin: Col. 6, Lines 34-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a processor as taught by Aslin to the fault condition of Ulybin because the consolidation module generates an isolated fault from the fault data by screening out cascaded faults and consolidating multiple faults (see Aslin: Col. 6, Lines 39-45).

As to dependent claim 28, Ulybin teaches a self-test method according to claim 26. Ulybin clearly teaches the electronic system, wherein the placing of the system into a first fault condition and subsequent reversion of the system to a non-fault condition (see Ulybin: Page 14, Third Paragraph), but does not mention a processor. Aslin

teaches operation of a processor (see Aslin: Col. 6, Lines 34-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a processor as taught by Aslin to the fault condition of Ulybin because the consolidation module generates an isolated fault from the fault data by screening out cascaded faults and consolidating multiple faults (see Aslin: Col. 6, Lines 39-45).

As to dependent claim 29, Ulybin teaches a self-test method according to claim 28. Ulybin clearly teaches the fault-monitoring device (see Ulybin: Page 3), but does not mention a voltage detector. Aslin teaches a voltage detector which generates a fault signal when an over-voltage occurs (see Aslin: Col. 12, Lines 38-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a voltage detector as taught by Aslin to the fault-monitoring device of Ulybin because the analog discrete fault data is analyzed in the same manner as the digital fault data (see Aslin: Col. 12, Lines 47-49).

As to dependent claim 30, Ulybin teaches a self-test method according to claim 28 wherein the fault-monitoring device comprises a device for monitoring the operation and generating a fault signal on detection of a fault with the operation (see Ulybin: Page 3), but does not mention a processor. Aslin teaches operation of a processor (see Aslin: Col. 6, Lines 34-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a processor as taught by Aslin to the fault-monitoring device of Ulybin because the consolidation module generates an isolated fault from the fault data by screening out cascaded faults and consolidating multiple faults (see Aslin: Col. 6, Lines 39-45).

As to dependent claim 31, the combination of Ulybin and Aslin teach a self-test method according to claim 28. Ulybin further teaches the self-test method comprising clearing the non-volatile memory of the record once it has been determined whether or not the non-volatile memory includes a record (e.g., when runs at the inputs of comparison block 3 do not match, its output shows the value "0," which is then recorded to trigger 4 by the signal from input 12) (see Page 9, Second Paragraph).

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tejal J. Gami whose telephone number is (571) 270-1035. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (571) 272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Anthony Knight
Supervisory Patent Examiner
Tech Center 2100

TJG

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